IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE)
e-ISSN: 2278-1676,p-ISSN: 2320-3331,
PP 43-50
www.iosrjournals.org

Multilevel Inverters-A Comparative Analysis

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Abstract: *The relevance of multilevel inverters has been increased since last few decades. These new types of inverters are suitable for high voltage and high power application. These inverters are able to synthesize waveforms with better harmonic spectrum and with less Total Harmonic Distortion (THD). Numerous topologies have been introduced and widely studied for utility of non-conventional sources and also for drive applications. This report presents information about several multilevel inverter topologies, such as the Neutral-Point Clamped Inverter and the Cascaded Multilevel Inverter. from among these some multilevel inverters will also be compared with a new topology with reduced number of switches. The THD values will also be compared. The modulation method used will be Sine PWM. The study will be mainly dealing with seven level inverter topologies.*

Keywords: *Multilevel, THD, Comparison, Sine PWM*

I. Introduction

Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generate voltages with stepped waveforms. The term multilevel starts with the three-level inverter introduced by Nabae et al[1]. By increasing the number of levels in the inverter, the output voltages have more steps that is, a staircase waveform, with reduced harmonic distortions. A multilevel inverter has several advantages over a conventional two-level inverter that uses high switching frequency pulse width modulation (PWM). The main attractive features of a multilevel inverter are[1] :

1) **Low dv/dt stress**: Multilevel inverters not only can generate the output voltages with very low distortion but also can reduce the dv/dt stresses.

2) **Common-mode (CM) voltage**: Multilevel inverters produce smaller CM voltage; therefore, the stress in the bearings of a motor connected to a multilevel motor drive can be reduced.

3) **Input current**: Multilevel inverters can draw input current with low distortion.

4) **Switching frequency**: Multilevel inverters can operate at both fundamental frequency and high switching frequency PWM. It should be noted that lower switching frequency usually means lower switching loss and higher efficiency.

Multilevel inverters do have some disadvantages. One being the requirement of many power semiconductor switches. Also each switch requires a related gate drive circuit. This may cause an increase in overall expenses of the system.

II. Multilevel Inverter Topologies

Multilevel inverters can be mainly divided into three major types:

1) *Cascaded H-bridge multilevel inverters*: These inverters include several H-bridge cells (Full-bridge inverters) connected in series.

2) *Diode-clamped multilevel inverters*: These inverters use clamped diodes and dc capacitors in order to generate ac voltage.This structure is known as neutral-point clamped (NPC) and is widely used in medium voltage, high power drives.

3) *Flying-capacitor multilevel inverter*: In this topology, semiconductor devices are in series and their connecting points are clamped by extra capacitors.

2.1. Cascaded H-bridge Multilevel Inverter

A structure of an m-level cascaded inverter is shown in Fig.1. Each separate dc source (SDCS) is connected to a H bridge inverter.The number of output phase voltage levels, *m*, is given by $m = 2s+ 1$, where s is the number of separate dc sources[2]. Cascaded inverters have been used for such applications as static var generation, with renewable energy sources, and in battery-based applications. The main advantages and disadvantages can be listed as[4] :

Advantages:

•The number of possible output voltage levels is more than twice the DC sources ($m = 2s + 1$).
• The series of H-bridges shows a modularized layout and packaging. This will enable the manufacturing process to be more quickly and cheaply.
• Possibility of soft-switching.
• Simple voltage balancing.

Disadvantages:
• Separate DC sources are required for each of the H bridges. This will limit its application to products that already have multiple SDCSs readily available.
• No common DC-bus.

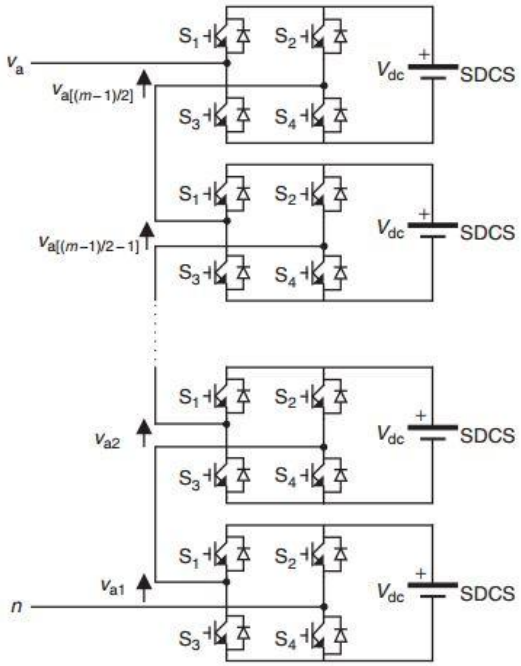

Fig. 1. Structure of a multilevel cascaded H-bridge inverter[2]

2.2. Neutral point clamped Multilevel Inverter[4],[5],[8],[9]

A common DC-bus is divided by bulk capacitors in series with a neutral point in the middle of the line. The number of capacitors depends on the number of voltage levels in the inverter. From this DC-bus, with neutral point and capacitors, there are clamping diodes connected to an ($m - 1$) number of switch pairs, where m is the number of voltage levels in the inverter.

One application of the multilevel diode-clamped inverter is an interface between a HV dc line and an ac line. Another would be a variable speed drive for high-power mediumvoltage motors. The main advantages and disadvantages of this inverter as as follows:

Advantages[8]:
• All the phases share a common dc bus, which minimizes the capacitance requirements of the converter.
• The capacitors can be precharged as a group.
• Efficiency is high for fundamental frequency switching
Disadvantages:
• Real-power flow is difficult for a single inverter.
• The number of clamping diodes required is quadratically related to the number of levels.

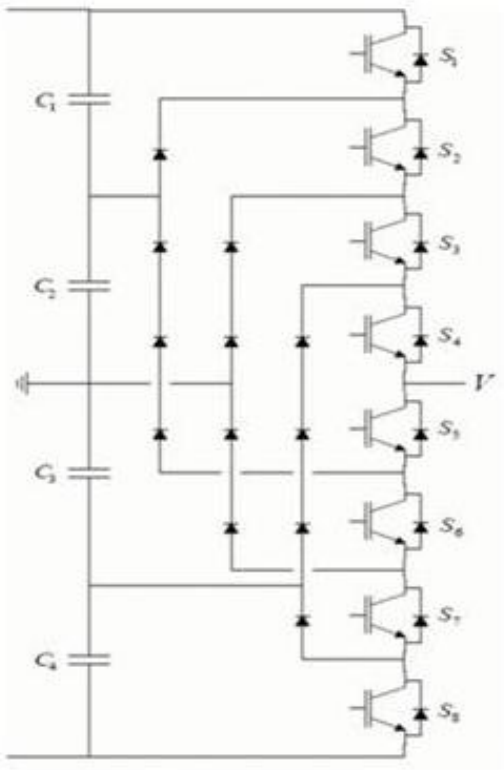

Fig. 2. Seven level diode clamped inverter[5]

2.3. Flying-capacitor Multilevel inverter[4],[7]

The structure of this inverter is similar to that of the diode-clamped inverter.Only difference is that instead of using clamping diodes, the inverter uses capacitors. The voltage on each capacitor differs from that of the next capacitor. The voltage increment between two adjacent capacitor legs gives the size of the voltage steps in the output waveform. The voltage synthesis in a seven-level capacitor-clamped converter has more flexibility than a diode clamped converter.

Similar to neutral point clamped inverter, the capacitor clamped inverter requires a large number of bulk capacitors of voltage clamping. The voltage rating of each capacitor used will be the same as that of the main power switch, therefore, an m-level converter will require a total of $(m-1)(m-2)/2$ clamping capacitors per phase leg in addition to $(m-1)$ main DC-bus capacitors. The advantages and disadvantages of capacitor clamped inverters are given below[4].

Advantages:

• Phase redundancies are available for balancing the voltage levels of the capacitors.
• Real and reactive power flow can be controlled.
• The large number of capacitors means the inverter can ride through short duration outages and deep voltage sags.

Disadvantages:

• Control is complicated to observe the voltage levels for all of the capacitors.Pre charging all of the capacitors to the same voltage level and startup are complex.
• Switching utilization and efficiency are poor for real power transmission.
• The more number of capacitors are both more expensive and bulky than clamping diodes in multilevel diodeclamped converters. Packaging is also more difficult in inverters with a high number of levels.
• Complicated control, leading to high switching frequency and losses, when transferring real power.

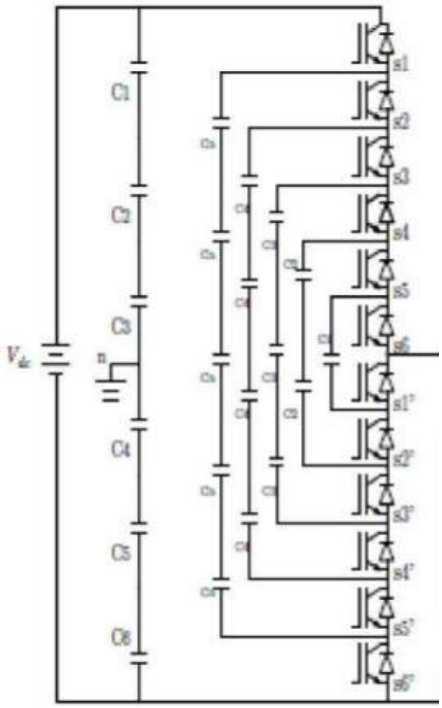

Fig. 3. Seven level capacitor clamped inverter

2.4. A New Topology with Reduced number of Switches[3]

Figure 4 shows the proposed novel topology used in the seven level inverter. An input voltage divider is composed of three series capacitors C1, C2, and C3. The divided voltage is given to H-bridge by four MOSFETs, and four diodes. The voltage is send to output terminal by H-bridge which is formed by four MOSFETs. The proposed multilevel inverter generates seven-level ac output voltage with the appropriate gate signals design. The purpose of the multilevel topology is to reduce the voltage rating of the power switch. By combining output voltages in multilevel form,shows advantages of low dv/dt, low input current distortion, and lower switching frequency. The major feature of the proposed topology is the reduction of power components.

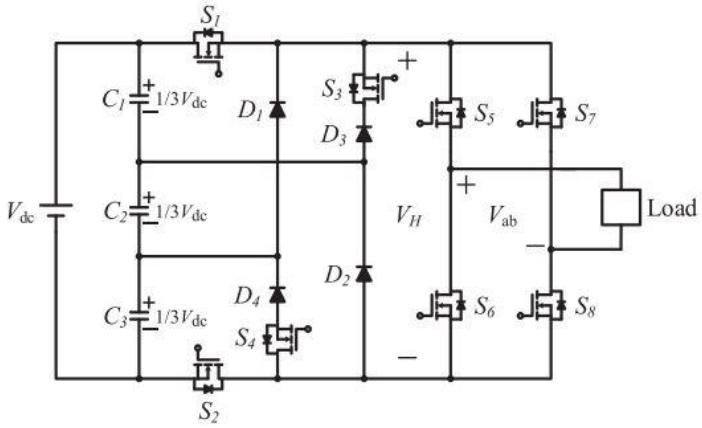

Fig. 4. Seven level Inverter with reduced number of switches[3]

III. Topology Comparison

Comparison of multilevel inverter is made based on the following criterias[9]:

- Number of semiconductor devices used per phase leg.
- Number of DC bus capacitors used.
- Number of voltage balancing capacitors used per phase.
- Amplitude of fundamental and effective harmonic components.
- Total Harmonic Distortion of output voltage.
- Control complexity based on voltage unbalances of

power switches.
• Cost estimation in designing of power circuit and the associated components.

Topology	Diode clamped	Capacitor clamped	Cascaded
Power Semiconductor switches	2(m-1)	2(m-1)	2(m-1)
Clamping diodes per Phase	(m-1)(m-2)	0	0
DC bus capacitor	(m-1)	(m-1)	(m-1)/2
Balancing capacitor per phase	0	(m-1)(m-2)/2	0
Voltage Unbalancing	Average	High	Very small

Table 3.1 Comparison of different multilevel inverter topologies

By comparing the number of devices needed, it can be seen that the proposed topology has much less number than the others.

Devices	New Topology	Diode clamped	Capacitor clamped	Cascaded
Input Sources	1	1	1	3
Input capacitors	3	6	2	3
Clamped capacitor	0	0	5	0
Power switches	8	12	12	12
Diodes	4	10	0	0

Table 3.2. Comparison of number of devices

IV. Simulation And THD Analysis

Simulation of two of the aforementioned topologies were done using MATLAB SIMULINK and the Total Harmonic distortion was analysed and compared.

1) Cascaded H bridge topology: The simulation diagram of Cascaded H-bridge topology is shown in Fig.5 and its output waveform is shown in Fig.6.

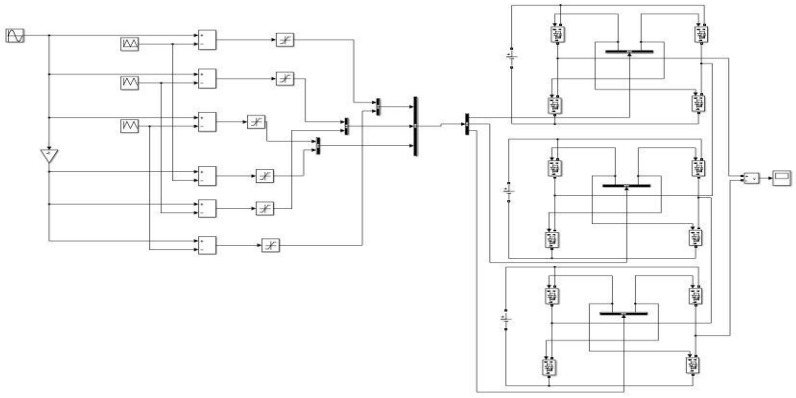

Fig. 5. Simulation model of cascaded multilevel topology

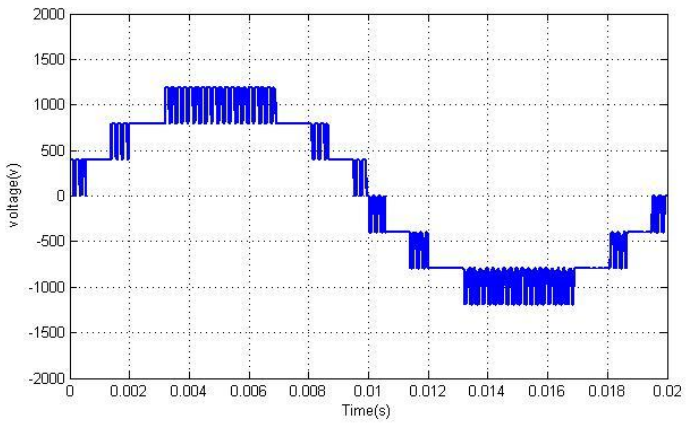

Fig. 6. Output voltage with seven levels of cascaded MLI

The THD analysis gave results as follows :

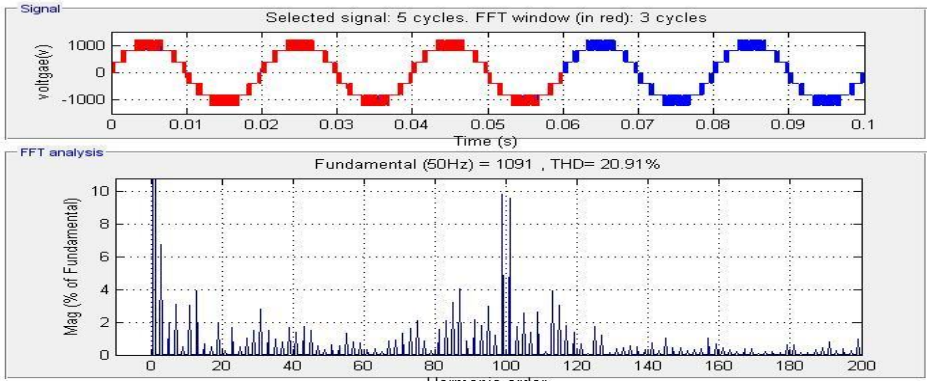

Fig. 7. THD analysis of cascaded H bridge topology

3)Neutral point clamped topology:

The simulation of a single phase neutral point clamped mli topology was done and the following wave form was obtained.

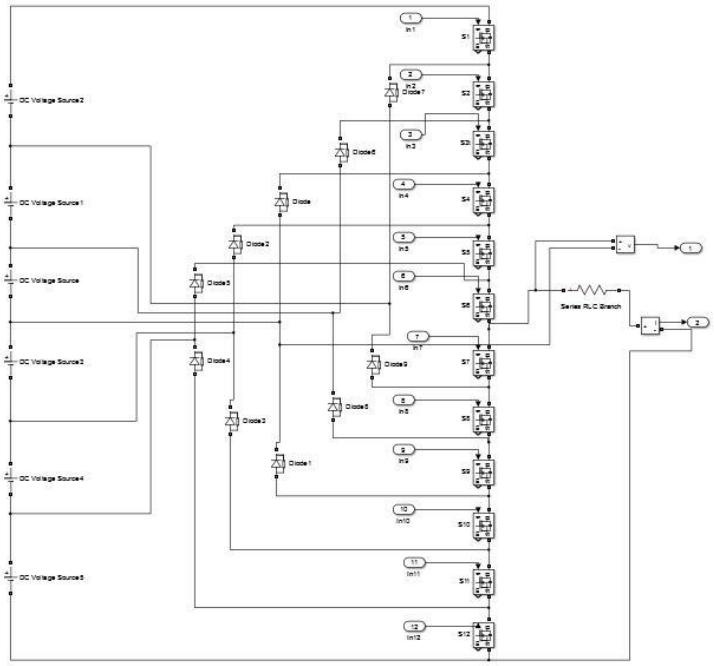

Fig 8. Simulink model of NPC MLI

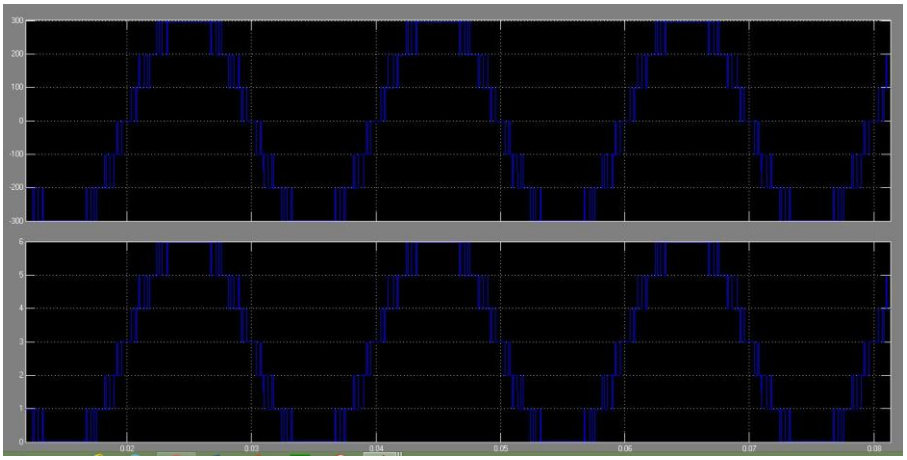

Fig 9. Output voltage waveform with seven levels for NPC MLI

The THD analysis is as shown below:

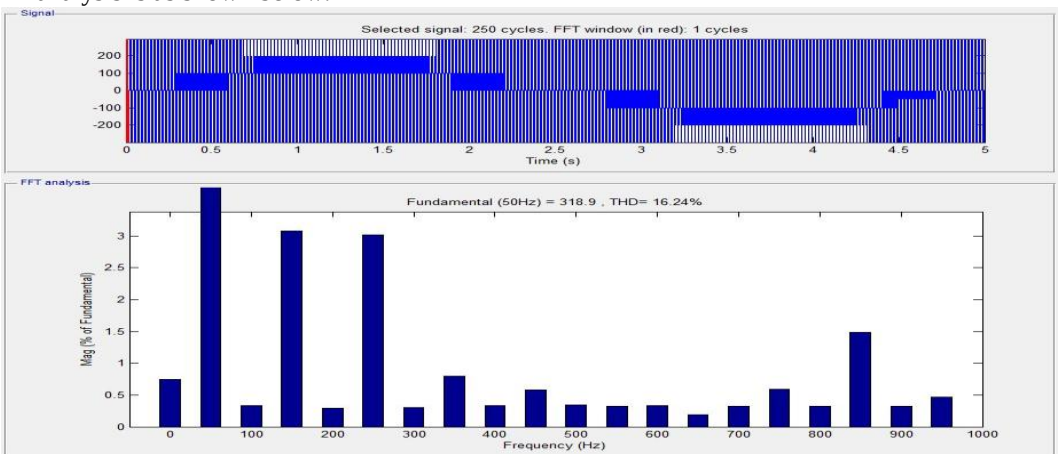

Fig 10. THD analysis of NPC MLI

2) Seven level topology with reduced number of switches:

The simulation of a new seven level topology was done and compared with the other topologies.

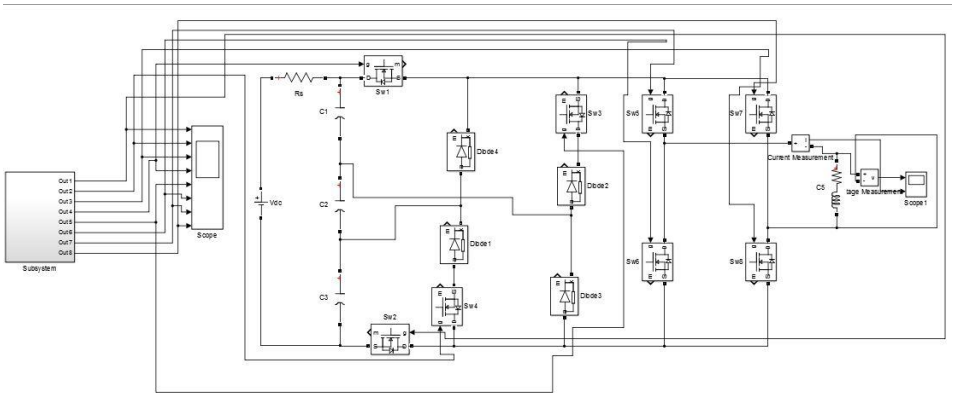

Fig. 8. Simulation model of new topology with less number of switches

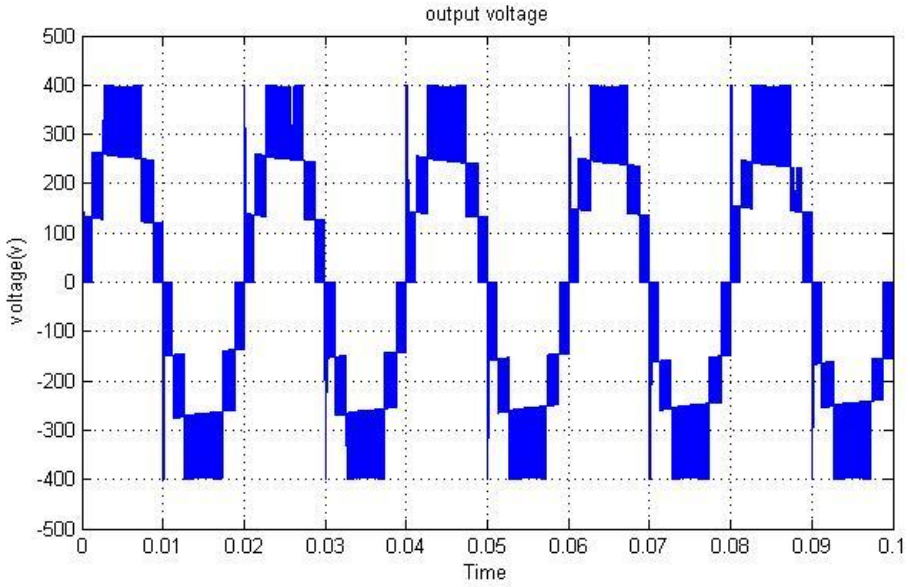

Fig. 9. Output voltage of new topology with seven levels

The THD analysis of this topology is shown below:

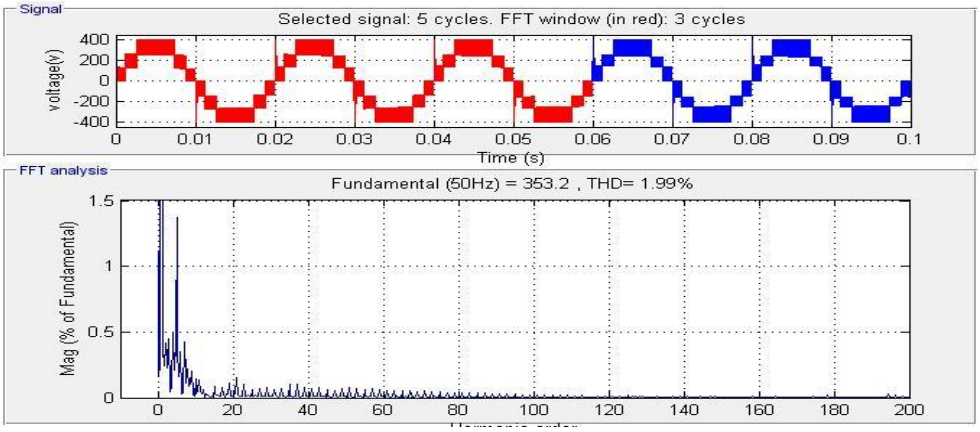

Fig. 10. THD analysis of New topology

Topology	Cascaded H bridge	Neutral point clamped	New topology
THD %	20.91	16.24	1.99

V. Conclusion

Various Multilevel inverter topologies were studied using simulation results. The THD analysis revealed that as number of levels increase the harmonic profile is improved. THD of the new topology with reduced number of switches was found to be the lowest, thereby making it the better topology among others.

References

[1] J. Rodriguez, J.-S. Lai, and F. Z. Peng, *Multilevel inverters: a survey of topologies, controls, and applications*, *IEEE Transactions on Industrial Electronics, vol. 49, no. 4, pp. 724 738, Aug 2002.*

[2] *Power electronics handbook*, Muhammad.H.Rashid,ISBN 978- 0-12-382036 5,2011 ,Elsevier Inc.

[3] Cheng-Han Hsieh, Tsorng-Juu Liang, ShihMing Chen,, IEEE, and ShihWen Tsai,*Design and Implementation of a Novel Multilevel DCAC Inverter,IEEE Transactions on industry applications, vol. 52, no.3 may/june 2016*

[4] Mohammadreza Derakhshanfar,*Analysis of different inverter topologies*,Thesis report,Department of Energy and Environment Division of Electric Power Engineering Chalmers University of Technology SE-412 96 Gteborg Sweden.

[5] Andreas Nordvall, *Multilevel Inverter Topology Survey*,Thesis Report,Department of Energy and Environment Division of Electric Power Engineering, Chalmers university of technology Gteborg, Sweden, 2011

[6] M. Murugesan, R.Pari, R.Sivakumar and S.Sivaranjani,*Different types of Multilevel Inverter Topologies-A Technical Review,International Journal of Advanced Engineering Technology,Vol. VII,Issue I,Jan.- March.,2016,149-155*

[7] *Flying Capacitor Multilevel Inverter*,http://engineering.electricalequipment.org/electrical distribution/ flying-capacitormultilevelinverters.html

[8] Jose Rodriguez, Steffen Bernet, Peter K. Steimer, and Ignacio E. Lizama,*A Survey on Neutral-Point-Clamped Inverters,IEEE transactions on industrial electronics , vol.57, no.7, july 2010*

[9] Lekha Sejpal,*Comparison of Two-level and Three-level Neutral-Point Clamped Inverters in automotive applications*,Thesis Report,Concordia University Montreal, Quebec, Canada,2013.

[10] Sanoop P., Vinita Chellappan,*Seven Level Inverter Topologies: A Comparative Study,International Journal of Innovative Research in Electrical, Electronics, Instrumentation and Control Engineering,Vol. 3, Special Issue 1, February 2016.*